SNIA Solid State Storage Initiative
PCIe SSD Task Force

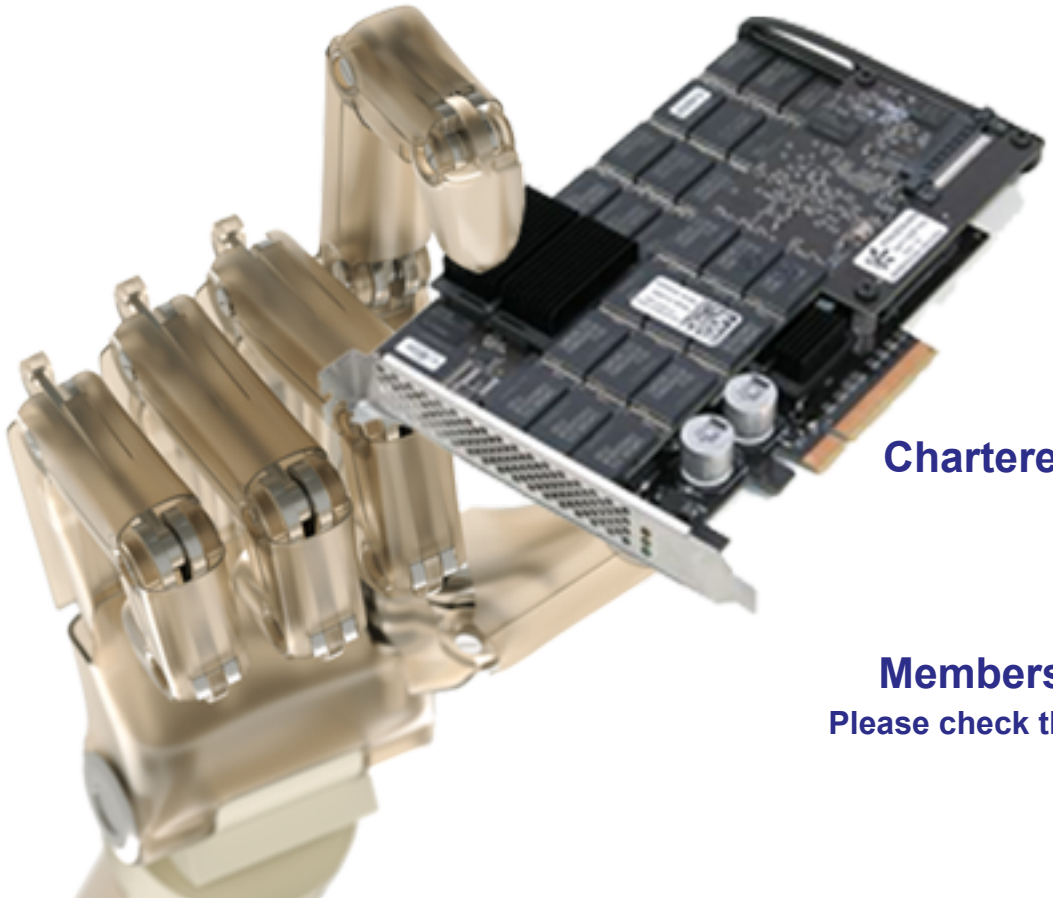
Meeting No. 1

Monday 09 APR 2012

WELCOME!

SNIA
Advancing storage & information technology

Kick-Off Meeting
Monday 09APR2012
4:00 PM - 5:30 PM PST



Welcome to the SNIA
Solid State Storage Initiative

PCIe SSD Task Force

This is an Industry Task Force
Chartered to investigate, discuss & educate
All things PCIe SSD

Membership is Complimentary for (90) Days
Please check the homepage at www.snia.org/forums/sssi/pcie

Task Force Participants

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Concall Guidelines:

- Use your mute button
- Be on time for roll call
- Un Mute when talking
- Use webex chat to ask questions
- Respond to Feedback Requests
- Email String Topic Discussions
- Email comments to reflector
  pciessd@snia.org
- Send Questions to
  pciechair@snia.org

(8) OPEN Meetings - Apr - Jul
SSSI Committee Aug - Dec 2012

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Topics	09APR12 OPEN	23APR12 OPEN	07MAY12 OPEN	21MAY12 OPEN	04JUN12 OPEN	18JUN12 OPEN	02JUL12 OPEN	16JUL12 OPEN	30JUL12 SSSI Committee
Kick-Off Mtg Issue Identification	X								
Standards		X							
Test Platforms		X							
Performance			X						
System Integration			X						
Other tbd									

Goals: Issue Identification & Committee 2012 Roadmap

Time: 4:00 – 4:05

AGENDA – 09 APR 12

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I.	**Administrative**	
a.	Roll Call; Call Schedule	4:00 – 4:05
b.	Announcements; Other	4:05 - 4:15
II.	**Business**	
a.	**Introduction & Welcome**	4:05 – 4:15
b.	**PCIe SSD Initial Survey Review**	4:15 - 4:35
c.	**PCIe 101 - Industry Overview**	4:35 - 4:50
d.	**Introduction to Topics of Interest**	4:50 - 5:20
III.	**Open**	
a.	Discussion	5:20 – 5:30
b.	Close	

Time: 4:00 – 4:05

Attendance

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Company	09APR12	23APR12	07MAY12	21MAY12	04JUN12	18JUN12	02JUL12	16JUL12
Agilent	x							
Allion	x							
AMD	x							
Apacer								
Cadence	x							
Calypso	x							
Cisco								
CLabs								
Corsair								
Coughlin Associates	x							
Dell	x							
eAsic	x							
EMC	x							
Enmotus	x							
eTron								
Fusion-io	x							
HDS	x							
HP	x							
HGST	x							

Time: 4:00 – 4:05

Attendance

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Company	09APR12	23APR12	07MAY12	21MAY12	04JUN12	18JUN12	02JUL12	16JUL12
Huawei	x							
HyperIO	x							
IBM	x							
Intel	x							
Lecroy								
Lenovo	x							
Lotes								
LSI	x							
Marvell	x							
Micron	x							
Molex	x							
Mushkin								
Objective Analysis	x							
OCZ	x							
Oracle	x							
Phison	x							
Renesas	x							
Samsung	x							
Sandisk	x							

Time: 4:00 – 4:05

Attendance

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Company	09APR12	23APR12	07MAY12	21MAY12	04JUN12	18JUN12	02JUL12	16JUL12
Seagate	x							
Smart Storage								
SNIA	x							
STEC	x							
Taejin	x							
Tektronix								
TMS	x							
Toshiba								
Tyco Electronics	x							
Unigen	x							
Viking								
Virident								
WDC	x							

Time: 4:00 – 4:05

Introduction

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1. Welcome: Eden Kim, Chair
   a. SSSI PCIe SSD Task Force Charter
   b. Task Force Deliverables
   c. Task Force Structure

2. SNIA Overview: Paul Wassenberg, Chair
   a. SNIA Org Chart
   b. SSSI Org Chart
   c. SSSI Programs & Projects
   d. SSS Performance Test Specification (PTS)

Time: 4:05 – 4:15

Welcome

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Task Force Charter:

1. **Provide Guidance to Marketplace about PCIe SSDs**
    1. Educational Materials
    2. Best Practices Documents
    3. Industry Standards Work
2. **Coordinate w/ other Industry Organizations**
    1. Complement other groups
    2. Avoid Overlap
    3. Fill Voids
3. **Open Industry Forum to SSSI Committee**
    1. (90) Day Free Trial Membership
    2. SNIA SSSI Membership Required July 2012
    3. No IP/NDA - No Confidential Information may be discussed
    4. Identify Issues & Define Roadmap for Committee

Time: 4:05 – 4:15

Welcome

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Task Force Deliverables:

1. PCIe SSD Hardware Test Specification
    1. Reference Hardware Platform
    2. Refresh of SSSI RTP Specification (Gen 3 PCIe)
    3. Interfaces, form factors, drivers, test cards
2. PCIe SSD Specific Performance Issues
    1. Investigate Test Protocol Issues
    2. PCIe SSD Power Management
    3. Recommendations to SSS TWG for Standards
3. Overview of PCIe SSD Industry Standards
    1. Description & Comparison of PCIe Standards
    2. Table of Standards Groups
4. PCIe Industry Coverage
    1. PCIe Industry Survey
    2. Best Practices Documents
    3. PCIe Round Table Forum at Flash Memory Summit Aug 2012

Time: 4:05 – 4:15

Welcome

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Task Force Structure:

1. **Webex Meetings - Every other Monday**
    1. Starting Monday 09APR12 and every two weeks thereafter
    2. 4:00 PM - 5:30 PM PST
    3. (8) Open Calls prior to SNIA/SSSI Membership Requirement

2. **Email Reflector - pciessd@snia.org**
    1. Agenda, Minutes & Discussion via reflector until 16JUL12
    2. Post Meeting Survey's for feedback and agenda preparation
    3. Email reflector becomes SSSI member only starting 16JUL12

3. **Target Objectives for (90) Day Public Forum Period**
    1. Table of Standards Groups
    2. Recommendation on PCIe Hardware Test Platform Standard
    3. Identification of PCIe SSD Performance Issues
    4. Hosting of PCIe Round Table Panel
    5. Other Objectives defined by Task Force
    6. Identity Issues & Recommend SSSI PCIe Committee Roadmap for 2012

Time: 4:05 – 4:15

SNIA Overview

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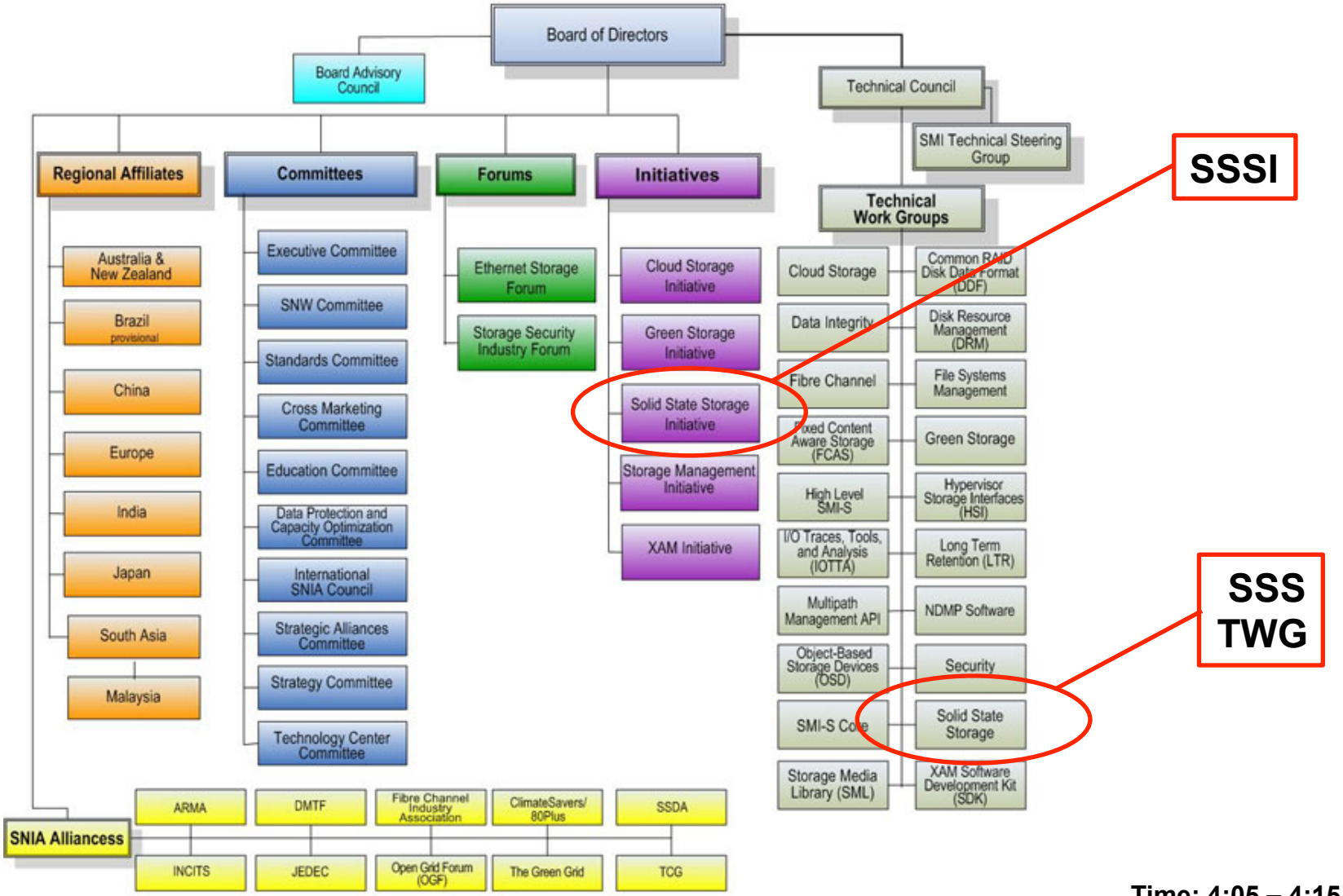

Storage Networking Industry Association • Governance & Committee Structure • October 2011

Time: 4:05 – 4:15

SSSI / SSS TWG Overview

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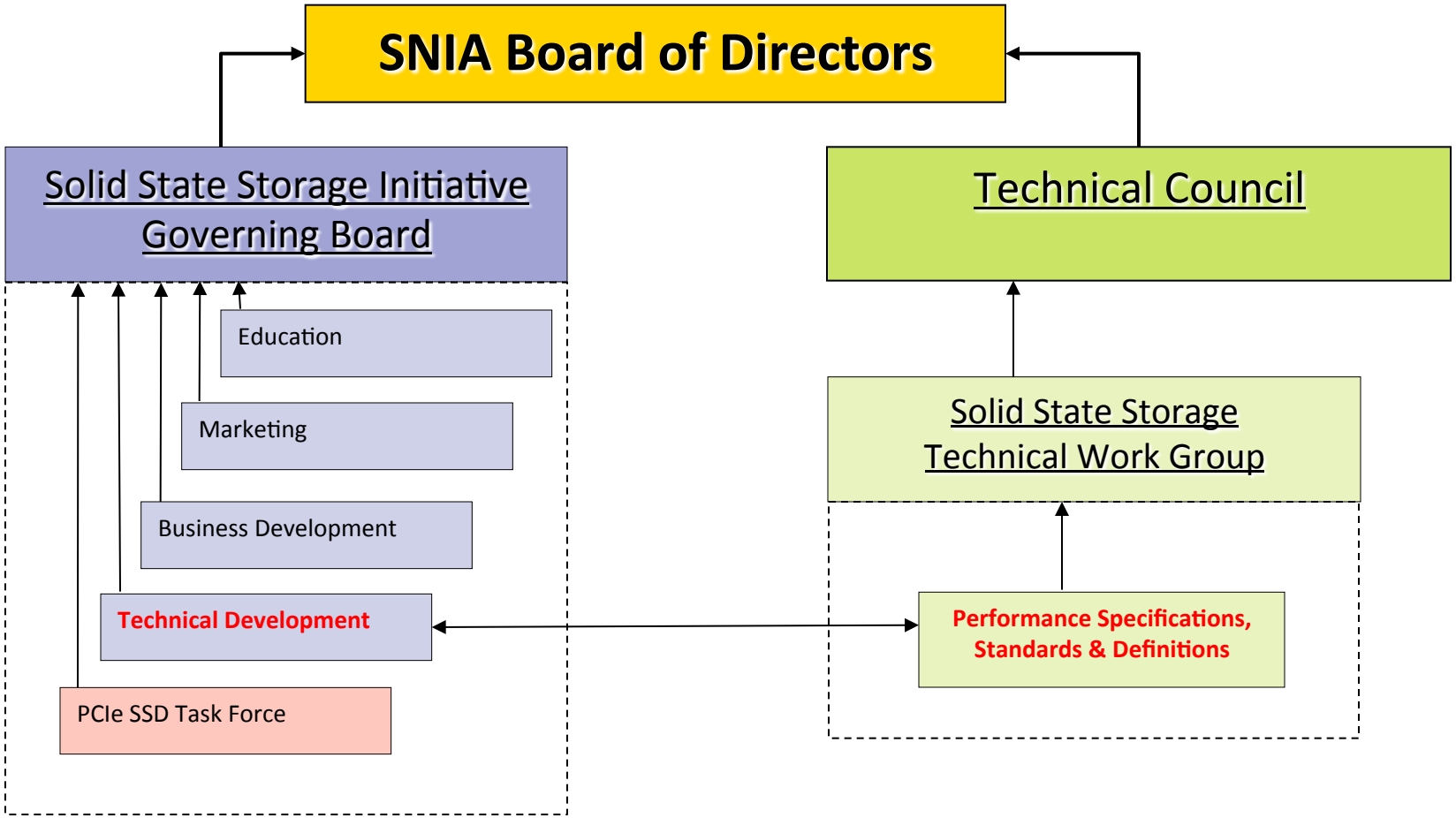

Time: 4:05 – 4:15

SSSI Programs Overview

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- **SSSI homepage** www.snia.org/forums/sssi
- **Understanding SSD Performance Project** www.snia.org/forums/sssi/pts
- **SSS Performance Test Specification (PTS)** www.snia.org/pts
- **PTS Standard Report Format** www.snia.org/forums/sssi/pts
- **SSSI Bright Talk Webcasts** www.snia.org/forums/sssi/knowledge/education
- **SSSI White Papers** www.snia.org/forums/sssi/knowledge/education
- **PCIe SSD Task Force** www.snia.org/forums/sssi/pcie

Time: 4:05 – 4:15

Why SSSI?

- We've been asked why SSSI is the right group for the PCIe SSD Taskforce
- There are multiple groups involved in defining aspects of PCIe SSDs, but they are all focused on specific areas – Enterprise, Client, connectors, O/S driver interface, protocol, etc.
- The PCIe SSD Taskforce will provide the "big picture" – encompassing all aspects of PCIe SSD technology and covering all market segments
  - Fill in the gaps where necessary, either via liaison or SNIA standards
  - Save our members from having to participate in every group
- SNIA SSSI has alliances & members in common with all other groups involved in PCIe SSD standards
  - We will utilize their collateral as appropriate & keep their messaging
- SSSI is not pitching a particular I/O or connector or protocol
- Our goal is to provide objective information to enable intelligent choices

Time: 4:05 – 4:15

PCIe Survey Results
Q1: Rank Topics of Interest

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1. Please rank ALL the following issues based on level of importance to you. Create Chart

	Most	2	3	4	5	6	7	8	Least	Rating Average
PCIe Standards	**38.9% (21)**	25.9% (14)	18.5% (10)	7.4% (4)	3.7% (2)	0.0% (0)	0.0% (0)	3.7% (2)	1.9% (1)	2.41
PCIe Test Hardware Standard	16.7% (9)	**25.9% (14)**	24.1% (13)	3.7% (2)	13.0% (7)	3.7% (2)	7.4% (4)	1.9% (1)	3.7% (2)	3.43
Test Protocols	18.5% (10)	22.2% (12)	**27.8% (15)**	9.3% (5)	5.6% (3)	5.6% (3)	3.7% (2)	3.7% (2)	3.7% (2)	3.33
Product Architectures, Form Factors & Interfaces	**31.5% (17)**	27.8% (15)	20.4% (11)	3.7% (2)	11.1% (6)	3.7% (2)	0.0% (0)	0.0% (0)	1.9% (1)	2.57
PCIe Controller Issues	22.6% (12)	**28.3% (15)**	22.6% (12)	1.9% (1)	7.5% (4)	5.7% (3)	7.5% (4)	1.9% (1)	1.9% (1)	3.11
PCIe Drivers, System Integration Issues	**27.8% (15)**	25.9% (14)	20.4% (11)	11.1% (6)	7.4% (4)	0.0% (0)	3.7% (2)	1.9% (1)	1.9% (1)	2.80
Power & Performance Issues	**28.3% (15)**	26.4% (14)	17.0% (9)	11.3% (6)	9.4% (5)	0.0% (0)	3.8% (2)	1.9% (1)	1.9% (1)	2.83
Market Positioning & Deployment Issues	**22.6% (12)**	20.8% (11)	**22.6% (12)**	9.4% (5)	11.3% (6)	5.7% (3)	0.0% (0)	3.8% (2)	3.8% (2)	3.25
Other	15.0% (3)	20.0% (4)	10.0% (2)	5.0% (1)	10.0% (2)	0.0% (0)	5.0% (1)	5.0% (1)	**30.0% (6)**	5.00

Time: 4:15 - 4:35

PCIe Survey Results
Q1: Rank Topics of Interest

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Topic	Most	2d Most	Least
PCIe Standards	21	14	1
Prod Arch, FF & IF	17	15	1
Drivers / Sys Integration	15	14	1
Power & Performance	15	14	1
PCIe Controller Issues	12	15	1
Mkt Position / Deployment	12	11	2
Test Protocols	10	12	2
PCIe Test HW Standard	9	14	2
Other	3	4	1

- **"Other Topics" submitted:**
  - PCIe SSD enterprise cabling standards
  - NVMe v SOP (protocols)
  - SFF – 8639 Connector (electrical pin out convention)
  - Economy Proposition

Time: 4:15 - 4:35

Question 1: Topic Rankings

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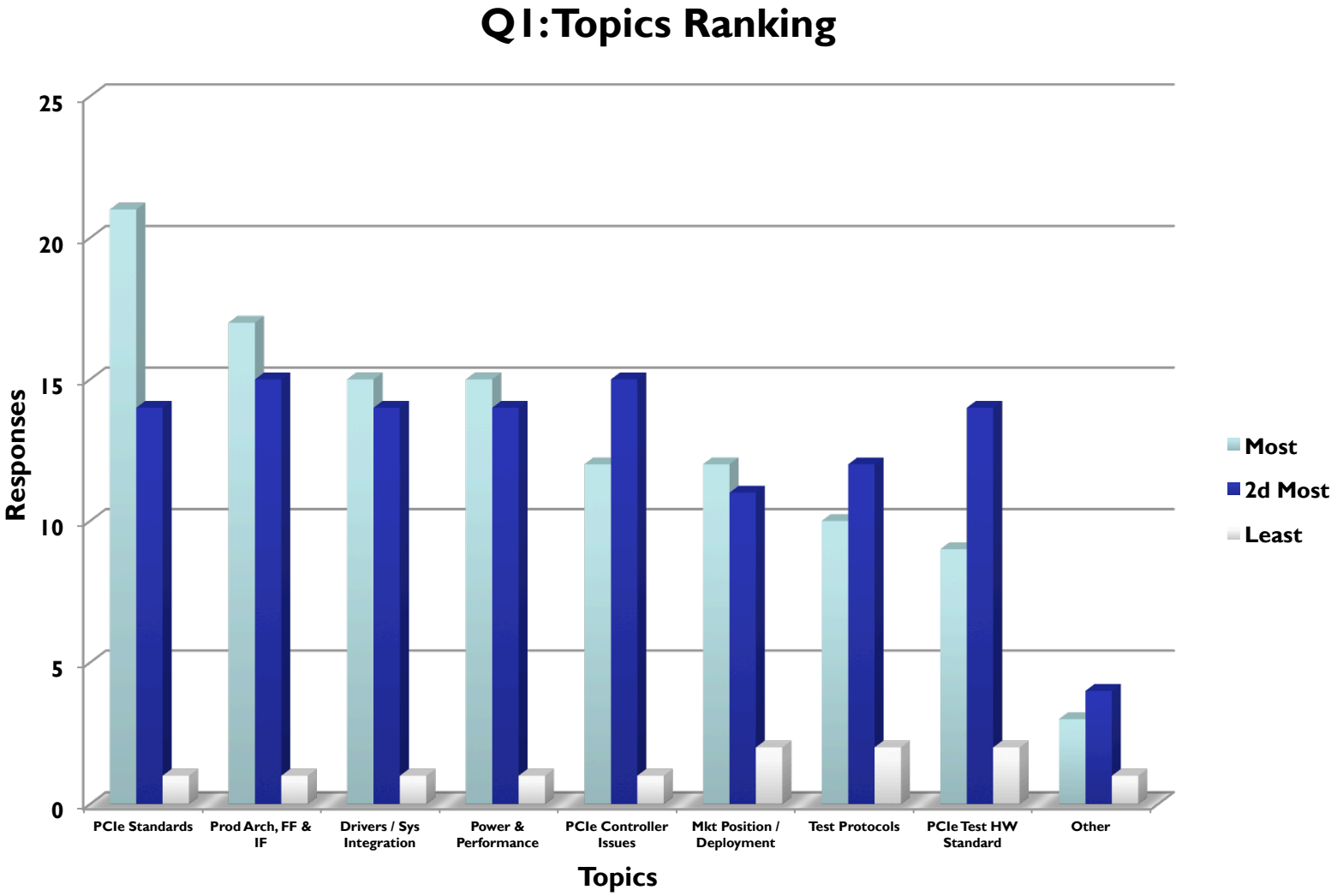

Time: 4:15 - 4:35

Question 2

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Please list the specific technical area(s) that interest you

- Performance:
  - Power/performance in NGFF to meet Ultrabook requirements
  - PCIe Performance – IOPS, TP & Latencies
  - Performance/Latency Market potential
  - Performance Workload matching
- Form Factor:
  - Mechanical SSD drive form factors
- PCIe interoperability;
  - PCIe3 and PCIe4 cabling (optics/CU)
  - Connector interface; Connector definition and requirements
- Standard's Technical requirement
  - Positioning of various PCI standards for storage access. PCI hot plug roadmap, guidelines.
  - Native PCIe SSD; Protocol Standards
  - SAS/PCIe integrated cabling. Software driver interfaces. Management interfaces.
  - Health Monitoring Feature
- Test requirement, logo compliance program
- Architecture Impact on traditioal storage PCIe DSS on server layer impact on storage design Meeting PCIe Standards PCIe SSD Performance OS Device drivers (Linux, Unix, Windows)

Time: 4:15 - 4:35

Question 3

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3. Task Force Goals: What do you most want the PCIe SSD Task Force to accomplish? (please rank ALL the following) Create Chart

	Most	2	3	4	5	6	7	Least	Rating Average
Identify PCIe Issues on an ongoing basis	29.8% (14)	**31.9% (15)**	17.0% (8)	14.9% (7)	0.0% (0)	2.1% (1)	2.1% (1)	2.1% (1)	2.49
Publish Task Force Technical Recommendations on Issues	25.5% (12)	**44.7% (21)**	19.1% (9)	8.5% (4)	0.0% (0)	0.0% (0)	0.0% (0)	2.1% (1)	2.23
Make Recommendations to the SSS TWG for Technical Standards Work	12.8% (6)	**42.6% (20)**	21.3% (10)	14.9% (7)	4.3% (2)	0.0% (0)	2.1% (1)	2.1% (1)	2.74
Make Recommendations to the SSSI for PCIe Market / Education Work	13.0% (6)	**34.8% (16)**	30.4% (14)	10.9% (5)	8.7% (4)	0.0% (0)	0.0% (0)	2.2% (1)	2.78
Create a permanent SSSI PCIe Committee	19.1% (9)	17.0% (8)	**23.4% (11)**	17.0% (8)	8.5% (4)	2.1% (1)	8.5% (4)	4.3% (2)	3.40
Create a SNIA PCIe Technical Working Group	19.1% (9)	23.4% (11)	**29.8% (14)**	12.8% (6)	0.0% (0)	8.5% (4)	2.1% (1)	4.3% (2)	3.06
Host PCIe Round Table Discussion at Industry Events	21.3% (10)	19.1% (9)	**23.4% (11)**	12.8% (6)	10.6% (5)	2.1% (1)	4.3% (2)	6.4% (3)	3.28
Other	0.0% (0)	0.0% (0)	0.0% (0)	25.0% (2)	0.0% (0)	0.0% (0)	0.0% (0)	**75.0% (6)**	7.00

Time: 4:15 - 4:35

Question 3

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What do you most want the PCIe SSD Task Force to accomplish?

Goals	Most	2d Most	Least
Ongoing Identification of PCIe Issues	14	15	1
PCIe Round Table Discussion at Industry Events	10	9	3
Publish Task Force Technical Recommendations	12	21	1
Create a permanent SSSI PCIe Committee	9	8	2
Recommendations to SSS TWG for Standards	6	20	1
Recommendations to SSSI for PCIe Market / Education	6	16	1
Create a SNIA PCIe Technical Working Group	9	11	2
Other	0	0	0

Time: 4:15 - 4:35

Question 3

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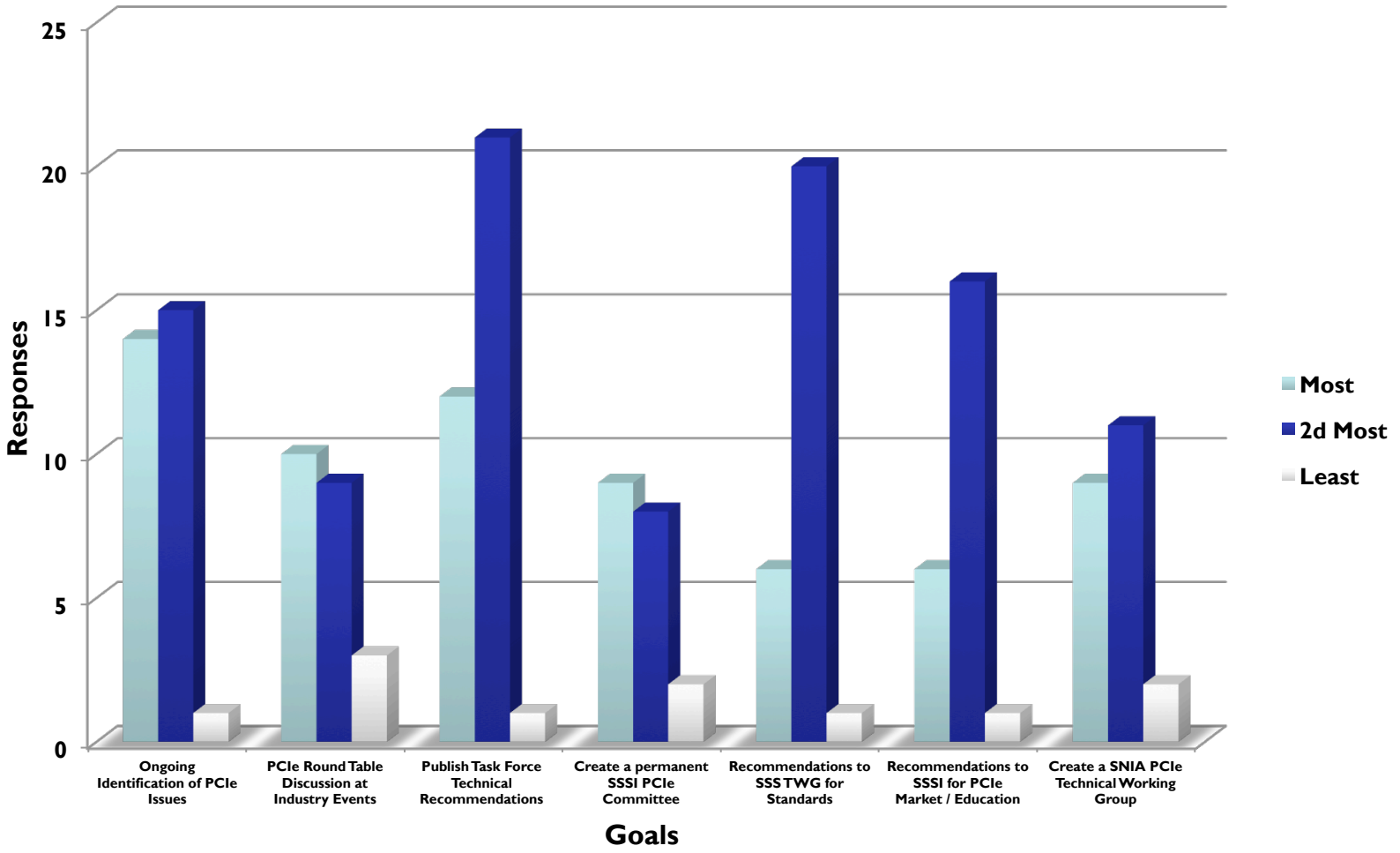
Q3: Goals You want the Task Force to Achieve



Time: 4:15 - 4:35

Question 4

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4. What take-aways and deliverables do you want from the PCIe SSD Task Force? (please rank ALL the following) Create Chart Download

	Most	2	3	4	Least	Rating Average	Response Count
Bi weekly concall / webex participation, minutes and investigations	33.3% (15)	**37.8% (17)**	22.2% (10)	4.4% (2)	2.2% (1)	2.04	45
Interaction / interface with PCIe SSD Task Force member companies and individuals	28.9% (13)	**42.2% (19)**	20.0% (9)	4.4% (2)	4.4% (2)	2.13	45
Creation of Task Force technical recommendations on Issues of Interest selected by the Task Force	24.4% (11)	**53.3% (24)**	20.0% (9)	0.0% (0)	2.2% (1)	2.02	45
Presentation of your company product / technology to the PCIe SSD Task Force participants	9.1% (4)	27.3% (12)	**31.8% (14)**	20.5% (9)	11.4% (5)	2.98	44
Other Deliverable(s) - please fill in comment box	10.0% (1)	10.0% (1)	10.0% (1)	0.0% (0)	**70.0% (7)**	4.10	10

Time: 4:15 - 4:35

Question 4

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What deliverables do you want from the PCIe SSD Task Force?

Deliverables	Most	2d Most	Least
Bi weekly concall / webex participation	15	17	1
Interaction / interface with Task Force members	13	19	2
Task Force technical recommendations	11	24	1
Your Company Presentation to Task Force	4	12	5
Other Deliverable(s)	1	1	7

Time: 4:15 - 4:35

Question 4

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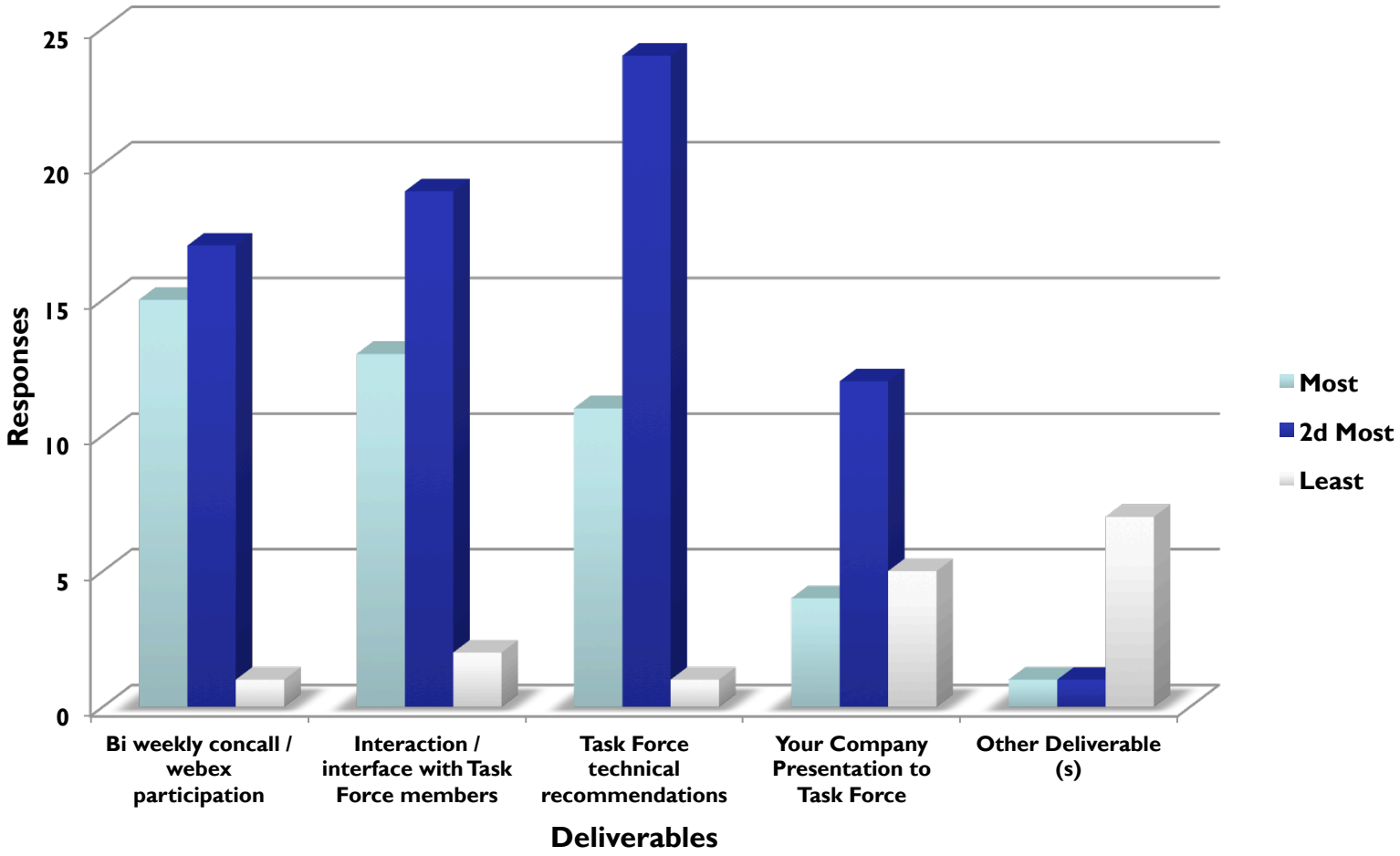
Q4: Task Force Deliverables



Time: 4:15 - 4:35

Question 5

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5. How much time and involvement do you wish / anticipate to make in the PCIe SSD Task Force? If you want a leadership role and to "Champion" an issue, please indicate the technical area/issue in the comment box. Create Chart Download

	Response Percent	Response Count
Minimum - one hour every other week for concall / webex meetings	**57.4%**	**27**
Active - additional participation on Issues of Interest	36.2%	17
Leadership - responsible for championing a specific Issue of Interest through the Task Force	6.4%	3
Other (please specify) Hide Responses		3

Time: 4:15 - 4:35

Question 6

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Questions for the Task Force Organizers?

- What is the strategy/roadmap?
- Need to understand the goals
- How will you influence the industry?
- How do you plan to interact/interplay with the other industry efforts to standardize on PCIe SSDs? Via representation, just adopt, try to drive convergence, etc.
- What is the area of focus for this WG?
- To get the justification of spending time for this Task Force, how PCIe SSD have the advantage than existing AHCI based SATA, SAS solution. If any other company have such comparison table showing, sharing could be better for this TF.

Time: 4:15 - 4:35

Question 7

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Questions for Kick Off Meeting?

- SATA Express proposal of support of only up to 2 lanes; does not support server backplane how will NGFF x2 and x4 PCIe support power requirements of Ultrabook?
- What are the goals, structure, deliverables, etc.
- How can you best leverage the massive list of task force members?
- What is the roadmap?
- How SNIA plans to drive standards convergence across the various independents and role in driving closure on important vendor implementation standards.
- What will this group cover that is not already covered by other WG's
- Please Define scope of SSSI PCIe Task Force

Time: 4:15 - 4:35

Question 9

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9. Which of the following best describes your company?	Create Chart	Download
	Response Percent	Response Count
PCIe OEM/mfgr/supplier	42.9%	15
PCIe vendor/distributor	20.0%	7
PCIe customer/user	5.7%	2
Industry participant	14.3%	5
Analyst	2.9%	1
Media / Press	0.0%	0
Internet Blog	0.0%	0
Other	14.3%	5
	Other (please specify) Show Responses	5

Time: 4:15 - 4:35

Question 11

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11. Where do you fit in the Storage hierarchy?	Create Chart
	Response Percent
SSD Flash tier	25.7%
PCIe SSD	**65.7%**
PCIe SATA-IO Express	22.9%
Other	28.6%

Time: 4:15 - 4:35

Topics of Interest

1. PCIe test hardware standards
2. Performance test protocols
3. Performance and reliability issues
4. Power management and performance
5. Controller configurations
6. Product architectures
7. Marketing issues
8. Deployment strategies
9. Industry standards

A brief discussion of Topics presented by select members follows.

Goal is to frame issues and solicit group feedback.

Slides will be the basis for more detailed discussion at future meetings.

Time: 4:50 - 5:20

PCIe 101
Introduction to PCIe Industry

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Overview:

Paul Wassenberg, Marvell

Marty Czekalski, Seagate

Time: 4:35 - 4:50

PCIe SSDs

Paul Wassenberg

- SSD interfaces are in danger of becoming a performance bottleneck
- SSDs are pushing current SATA and SAS interface speeds, and it's difficult for interfaces to keep up by following the traditional path of doubling the next generation of interface speeds
  - SAS is moving to 12Gb/s, but is not a permanent solution for high-end SSDs
  - SATA still at 6Gb/s
  - PCIe is a good fit for SSDs, as it allows the interface speed to be increased quickly by adding PCIe lanes
- PCIe as a mainstream SSD interface becomes economically feasible with Gen3 at 8Gb/s per lane
- SSDs on PCIe cards have been around for some time, but with mostly proprietary O/S drivers
- There are currently multiple groups focusing on standardizing SSDs in HDD-style form factors with a PCIe interface
  - Connector, protocol & driver interface standards enable interchangeability
  - Device interchangeability drives volume

Acronyms

- PCIe = PCI Express
- PCI-SIG – PCI Special Interest Group (controls PCIe spec)
- NVM = Non Volatile Memory (mainly NAND Flash today)
- NVMHCI = NVM Host Controller Interface (for client PCIe SSDs)
- NVMe = NVM Express (NVMHCI expanded to include enterprise)
- SOP = SCSI over PCIe (supports PQI and NVMe as queuing interfaces)
- PQI = PCIe Queuing Interface (referred to within SOP, similar in function to NVMe)
- SFF = Small Form Factor Committee (connector specifications); www.sffcommittee.com

Time: 4:35 - 4:50

PCIe SSD Standard Groups

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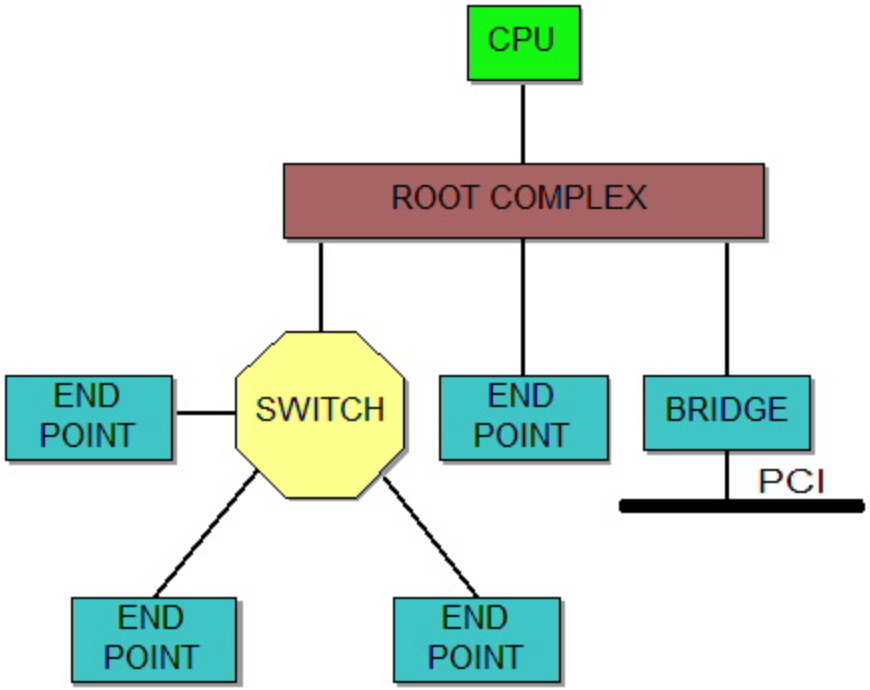
- NVM Express Group
  - Former NVMHCI team expanded PCIe SSD O/S driver interface to enterprise
  - v1.0 spec released in 2011; v1.1 with more enterprise features in 2012
- T10 (SAS/SCSI Standards Committee)
  - Developing SOP, which supports PQI & NVMe as queuing interfaces
  - Anticipate a stable spec within 2012
- SSD Form Factor Working Group
  - SFF-8639 multiprotocol connectors, hot plug, HDD-style form factor
  - Released v1.0 spec in late 2011
- SATA-IO (Client)
  - SATA Express – up to 2 lanes PCIe or 2 ports of SATA, connectors
  - Mainly connector development, expected to be released later in 2012
- SCSI Trade Association (Enterprise)
  - SCSI Express – based on T10 SOP/PQI and SSD FF WG work
  - SCSI Express announced as a project; more details coming in May

PCIe Topology

Marty Czekalski



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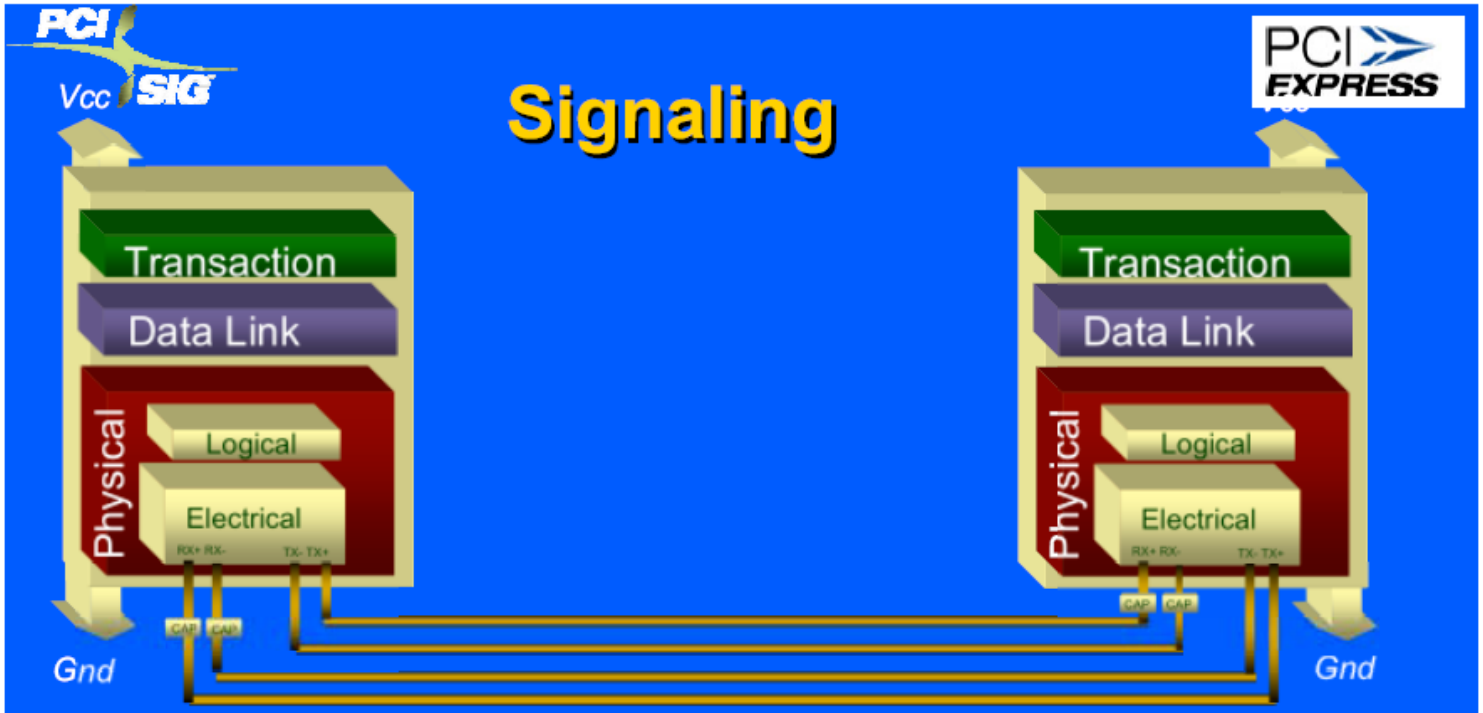
Time: 4:35 - 4:50

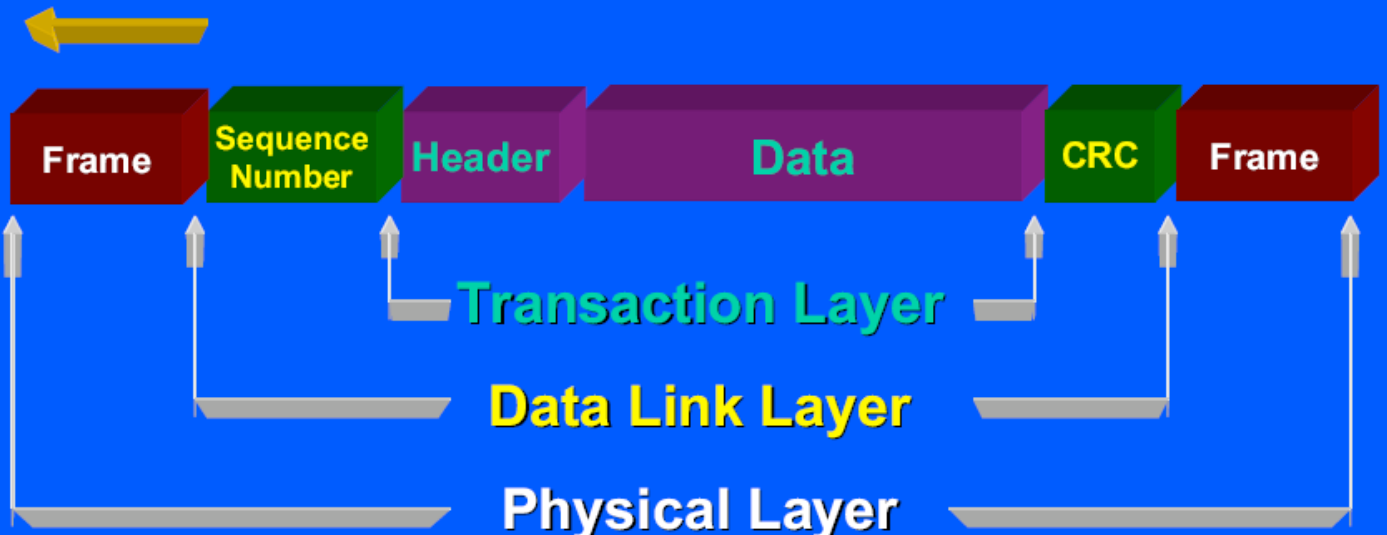
Signaling



- **Differential**
  - ✓ Superior voltage margins to single-ended
  - ✓ Voltage independence; VCC can vary
  - ✓ Reduces EMI problems
- **Serial Lanes**
  - ✓ Removes skew requirements between parallel lanes
  - ✓ Relaxed routing rules within a link
- **Routing length target**
  - ✓ 4 layer FR-4 boards; ~20 inches, 2 connectors

Time: 4:35 - 4:50

Packet Formation



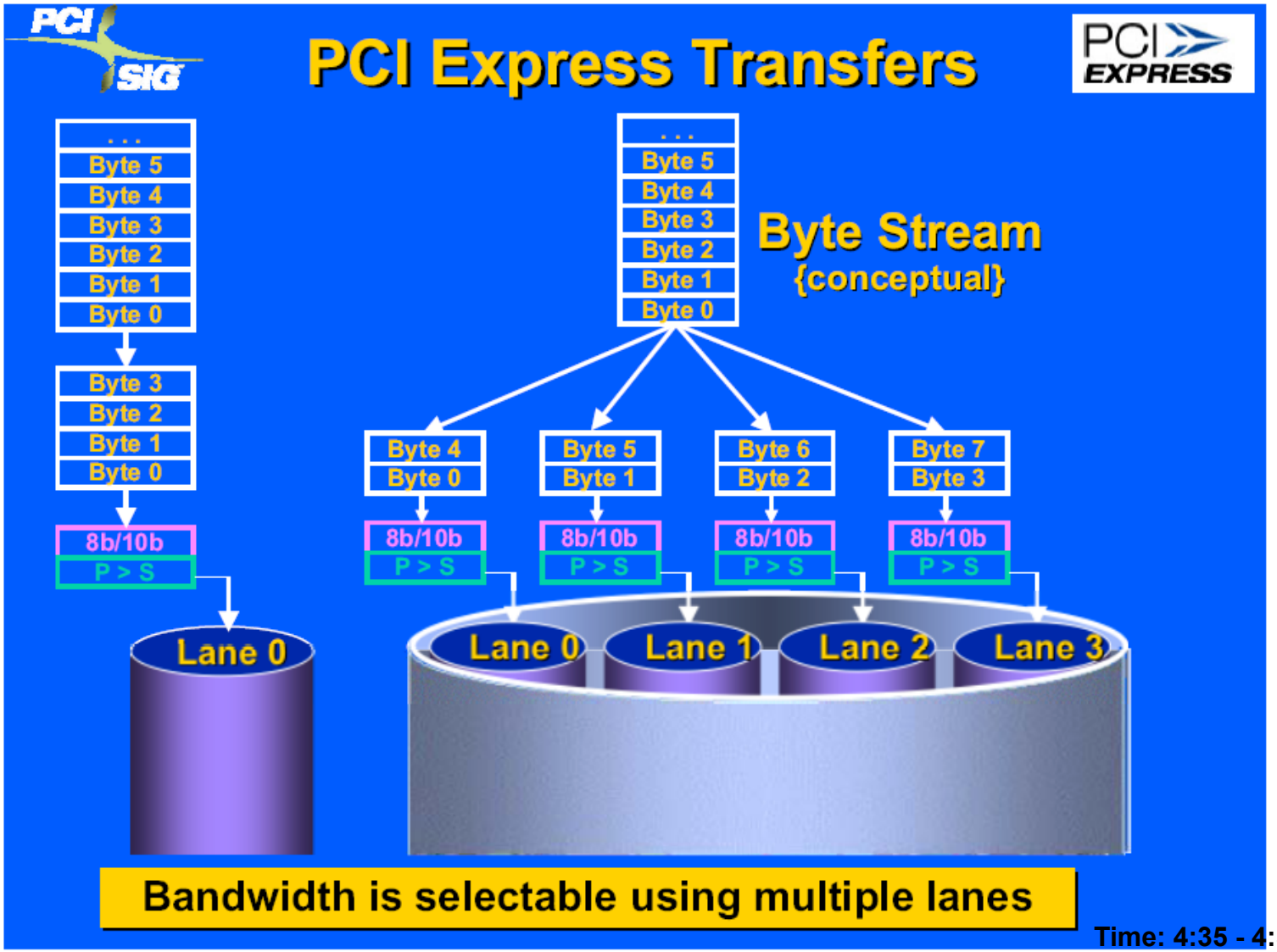
Formation of packets reflects layered architecture

Time: 4:35 - 4:50

PCIe Lanes

- PCIe connections are grouped into multiple lanes
  - Typically 1,4,8,16
  - A single operation utilizes all lanes in parallel for that transfer
    - SAS by comparison uses it's wide port links for concurrent operations across single links.

Time: 4:35 - 4:50


PCI SIG
PCI Express Transfers
PCI EXPRESS
. . .
Byte 5
Byte 4
Byte 3
Byte 2
Byte 1
Byte 0
Byte Stream
{conceptual}
Byte 3
Byte 2
Byte 1
Byte 0
8b/10b
P > S
Lane 0
Byte 4
Byte 0
Byte 5
Byte 1
Byte 6
Byte 2
Byte 7
Byte 3
Lane 0
Lane 1
Lane 2
Lane 3
Bandwidth is selectable using multiple lanes

Time: 4:35 - 4:50

PCIe Speeds

- Gen 1 – 2.5GT/sec = 250MB/sec/lane
  - 8b/10B
- Gen 2 – 5.0 GT/sec = 500MB/sec/lane
  - 8B/10B
- Gen 3 – 8 GT/sec = 1GB/sec/lane
  - 128B/130B
- Routing constraints have increased with each generation

Lots of additional form factors exist

Time: 4:35 - 4:50

Enterprise PCIe SSDs today

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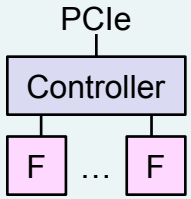
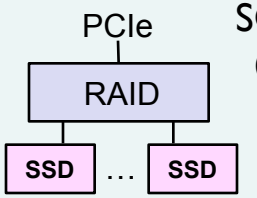
	Native	Aggregator
Commands/Transport	 Proprietary	 SCSI or SATA (Multiple SSDs & controller on card)
Committee	None	None
Standards Based	No	Yes
Performance with Flash	High	High
CPU Overhead	Low-High	Low
Latency with short queue	Very Low	Low
Latency with deep queue	Low-Moderate	Low
Use Case Extensibility	No	Yes (RAID, HBA, etc)
Maturity	Evolving	Based on Proven Industry Architectures
Enterprise feature set (PI, Security, Mgmt, etc.)	No	Depends on implementation

Time: 4:35 - 4:50

Enterprise SSD Form Factor

- New serviceable slot for PCIe attached devices
  - Also supports SAS in the same bay
- Specification available at SSDformfactor.org

Time: 4:35 - 4:50

"Express Bay" - Multi-function Bay

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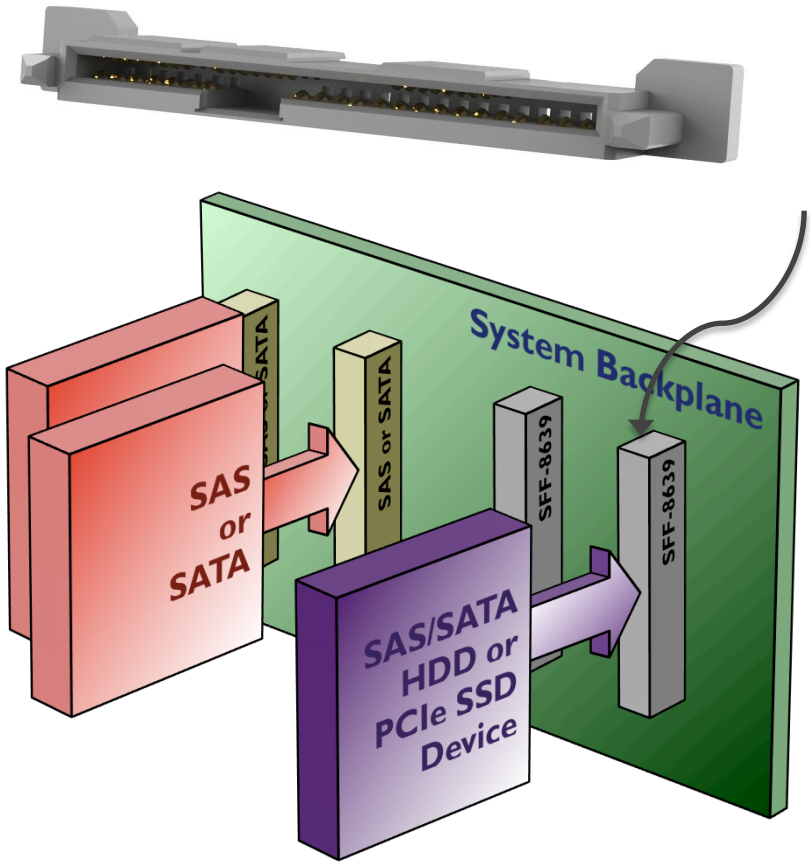
Multi-function SAS/PCIe bay

- Uses SFF-8639 Multi-function connector
- High performance (up to 25W per slot)
- Hot swap, serviceability (SAS)
- High availability (2 fault domains)
- Supports a range of devices

  (system dependent)
  - 12Gb/s SAS
  - PCIe SSDs (emerging)
    - NVMe, SOP-PQI, Proprietary
  - 6Gb/s SATA
  - MultiLink SAS (4 SAS Ports)
  - SATA Express

Multi-function Connector



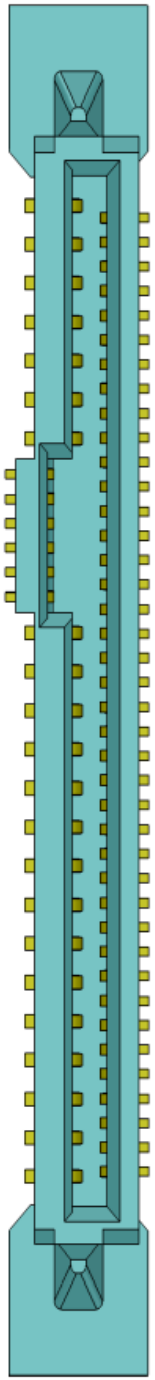
Time: 4:35 - 4:50

SFF-8639 Signals

Drive	Usage	Signal Description	Name	Mating	Pi
		Ground	GND	2nd	S
input	SAS+SATA	SAS/SATA/SATAe 0 Tx+	S0T+ (A+)	3rd	S
input	SAS+SATA	SAS/SATA/SATAe 0 Tx -	S0T- (A-)	3rd	S
		Ground	GND	2nd	S
output	SAS+SATA	SAS/SATA/SATAe 0 Rcv -	S0R- (B-)	3rd	S
output	SAS+SATA	SAS/SATA/SATAe 0 Rcv +	S0R+ (B+)	3rd	S
		Ground	GND	2nd	S
input	Dual Port	ePCIe RefClk + (port B)	RefClk1+	3rd	E
input	Dual Port	ePCIe RefClk – (port B)	RefClk1-	3rd	E
input	ePCIe opt	3.3V for SM bus	3.3Vaux	3rd	E
input	Dual Port	ePCIe Reset (port B)	ePERst1#	3rd	E
input	ePCIe	ePCIe Reset (port A)	ePERst0#	3rd	E
		Reserved	RSVD	3rd	E
input	SATAe +SAS4	Reserved(WAKE#/OBFF), SASAct2	RSVD(Wake#) /SASAct2	3rd	P
Bi-Dir	SATAe	SATAe Client /SAS reset	sPCIeRst/SAS	3rd	P
input	SATAe	Reserved (DevSLP#)	RSVD(DevSLP#)	2nd	P
output	SATAe + ePCIe	Interface Detect (Was GND-precharge)	IfDet#	1st	P
	all	Ground	GND	2nd	P
	all			2nd	P
NC	SAS+SATA	Precharge	5 V	2nd	P
NC	SAS+SATA	SATA, SATAe, SAS only		3rd	P
NC	SAS+SATA			3rd	P
	all	Presence (Drive type)	PRSNT#	2nd	P:
Bi-Dir	all	Activity(output)/Spinup	Activity	3rd	P:
	all	Hot Plug Ground	GND	1st	P:
input	all	Precharge	12 V	2nd	P:
input	all	All – 12V		3rd	P:
input	all	Only power for ePCIe SSD		3rd	P:

ePCIe → Enterprise PCIe (separate from SATA/SAS)

SATAe → SATA Express (Client PCIe- muxed on SATA/SAS signals)



Pin #	Mating	Name	Signal Description	Usage	Drive
E7	3rd	RefClk0+	ePCIe Primary RefClk +	ePCIe	input
E8	3rd	RefClk0-	ePCIe Primary RefClk -	ePCIe	input
E9	2nd	GND	Ground		
E10	3rd	PETp0	ePCIe 0 Transmit +	ePCIe	input
E11	3rd	PETn0	ePCIe 0 Transmit -	ePCIe	input
E12	2nd	GND	Ground		
E13	3rd	PERn0	ePCIe 0 Receive -	ePCIe	output
E14	3rd	PERp0	ePCIe 0 Receive +	ePCIe	output
E15	2nd	GND	Ground		
E16	3rd	RSVD	Reserved		
S8	2nd	GND	Ground		
S9	3rd	S1T+	SAS/SATAe 1 Transmit +	SAS+SATAe	input
S10	3rd	S1T-	SAS/SATAe 1 Transmit -	SAS+SATAe	input
S11	2nd	GND	Ground		
S12	3rd	S1R-	SAS/SATAe 1 Receive -	SAS+SATAe	output
S13	3rd	S1R+	SAS/SATAe 1 Receive +	SAS+SATAe	output
S14	2nd	GND	Ground		
E17	3rd	RSVD	Reserved		
E18	2nd	GND	Ground		
E19	3rd	PETp1/S2T+	ePCIe 1 /SAS 2 Transmit +	ePCIe+SAS4	input
E20	3rd	PETn1/S2T-	ePCIe 1 /SAS 2 Transmit -	ePCIe+SAS4	input
E21	2nd	GND	Ground		
E22	3rd	PERn1/S2R-	ePCIe 1 /SAS 2 Receive -	ePCIe+SAS4	output
E23	3rd	PERp1/S2R+	ePCIe 1 /SAS 2 Receive +	ePCIe+SAS4	output
E24	2nd	GND	Ground		
E25	3rd	PETp2/S3T+	ePCIe2 / SAS 3 Transmit +	ePCIe+SAS4	input
E26	3rd	PETn2/S3T-	ePCIe2 / SAS 3 Transmit -	ePCIe+SAS4	input
E27	2nd	GND	Ground		
E28	3rd	PERn2/S3R-	ePCIe 2 / SAS 3 Receive -	ePCIe+SAS4	output
E29	3rd	PERp2/S3R+	ePCIe 2 / SAS 3 Receive +	ePCIe+SAS4	output
E30	2nd	GND	Ground		
E31	3rd	PETp3	ePCIe 3 Transmit +	ePCIe	input
E32	3rd	PETn3	ePCIe 3 Transmit -	ePCIe	input
E33	2nd	GND	Ground		
E34	3rd	PERn3	ePCIe 3 Receive -	ePCIe	output
E35	3rd	PERp3	ePCIe 3 Receive +	ePCIe	output
E36	2nd	GND	Ground		
E37	3rd	SMClk	SM-Bus Clock	PCIe opt	Bi-DIr
E38	3rd	SMDat	SM-Bus Data	PCIe opt	Bi-Dir
E39	3rd	DualPortEn#	ePCIe 2x2 Select	Dual Port	input

From: SFF-8639 Rev. 0.5, January 3, 2012

Storage Interface Comparison

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	SATA	SAS		PCIe		
	SATA	SAS	Multilink SAS	SOP/PQI	NVM Express	Proprietary
Drive Form Factors	1.8", 2.5", 3.5"	2.5", 3.5"	2.5"	2.5"	2.5", Card	Card
No of Ports / Lanes	1	1, 2	1, 2, 4	1, 2, 4 (8 on card)	1, 2, 4 (8 on card)	1, 2, 4,8
Command Set / Queuing Interface	ATA / SATA-IO	SCSI / SAS	SCSI / SAS	SCSI / SOP / PQI	NVM Express	Vendor-Specific
Transfer Rate	6Gb/s	12Gb/s	12Gb/s	8 Gb/s	8 Gb/s	8Gb/s
Drive Connector	SATA-IO	SFF-8680	SFF-9630 SFF-8639	SFF-8639	SFF-8639 (2.5"), CEM (Edge-Card)	CEM (Edge-Card)
Express Bay Compatible?	Yes (2.5")	Yes (2.5")	Yes (2.5")	Yes (2.5")	Yes (2.5")	N/A
Drive Power	9W Typical (2.5")	9W Typical (2.5")	Up to 25W	Up to 25W	Up to 25W	Vendor Specific
Max Bandwidth	0.6 GB/s	4. 8 GB/s (x2)	9.6 GB/s (x4)	8 GB/s (x4)	8 GB/s (x4)	16GB/s (x8)
System and Use Case Considerations						
Host Driver Stack (Storage Controller / Direct Drives)	AHCI	IHV	IHV	Common Driver Possible (SOP/PQI)	Common Driver Possible (NVM Express)	IHV
Surprise Removal / Insertion ('Hot Plug')	Yes	Yes	Yes	Future Enhancement	Future Enhancement	Vendor Specific

Source: SCSI Trade Association

Time: 4:35 - 4:50

Other Topics of Interest

Easen Ho, Calypso - Test Protocols, Hardware & Standards

Hany Eskander, STEC - Design & Performance; Product Architectures & Form Factors

Tony Roug, Virident - SSD Architectures; Application Benefits of SSD Flash

Time: 4:50 - 5:20

Topics of Interest

Easen Ho, Calypso

- **Test Protocols**
- **Hardware Standard**

- **PTS-E & PTS-C set forth an RTP for Standardized, Normalized Performance Test of SSDs**
- **Existing RTP has Gen 2 PCIe 8 Lane Bus**
- **Refresh is needed for Gen 3 motherboards, active interposer boards, no. slots, power, etc.**
- **Other PCIe Specific Test Issues and Protocols need to investigated**

Time: 4:50 - 5:20

Topics of Interest

Hany Eskandar, STEC

•Design & Performance

- **Measuring the true performance with xGB of SDRAM on board**
- **Address the thermal affect due to double performance in Gen3**
- **Relax the requirement for data recovery, and out of band c/cs**
  - **Trades between switch scrambling, and 8b/10b encoding (relaxing**
- **Investigate the option of control or limit the PCIe card power consumption**
- **Advanced debug and test features include jitter injection for system margining, and automatic eye-diagram generation.**

•Product Architecture & Form Factors

- **Do we need enclosure case for PCIe?**
- **2.5” / 1.8” form factor**

Time: 4:50 - 5:20

Topics of Interest

Tony Roug, Virident

- **SSD Architectures**
  - **SSD management – e.g. interaction with OS storage tools linked to SCSI stack (e.g. Linux HDparm, Windows diskutils)**
  - **Reliability architectures especially for DAS on and across servers**
  - **Application architectures for accessing shared PCIe SSDs**
  - **Application architectures for optimizing to SSD performance**

Time: 4:50 - 5:20

Topics of Interest

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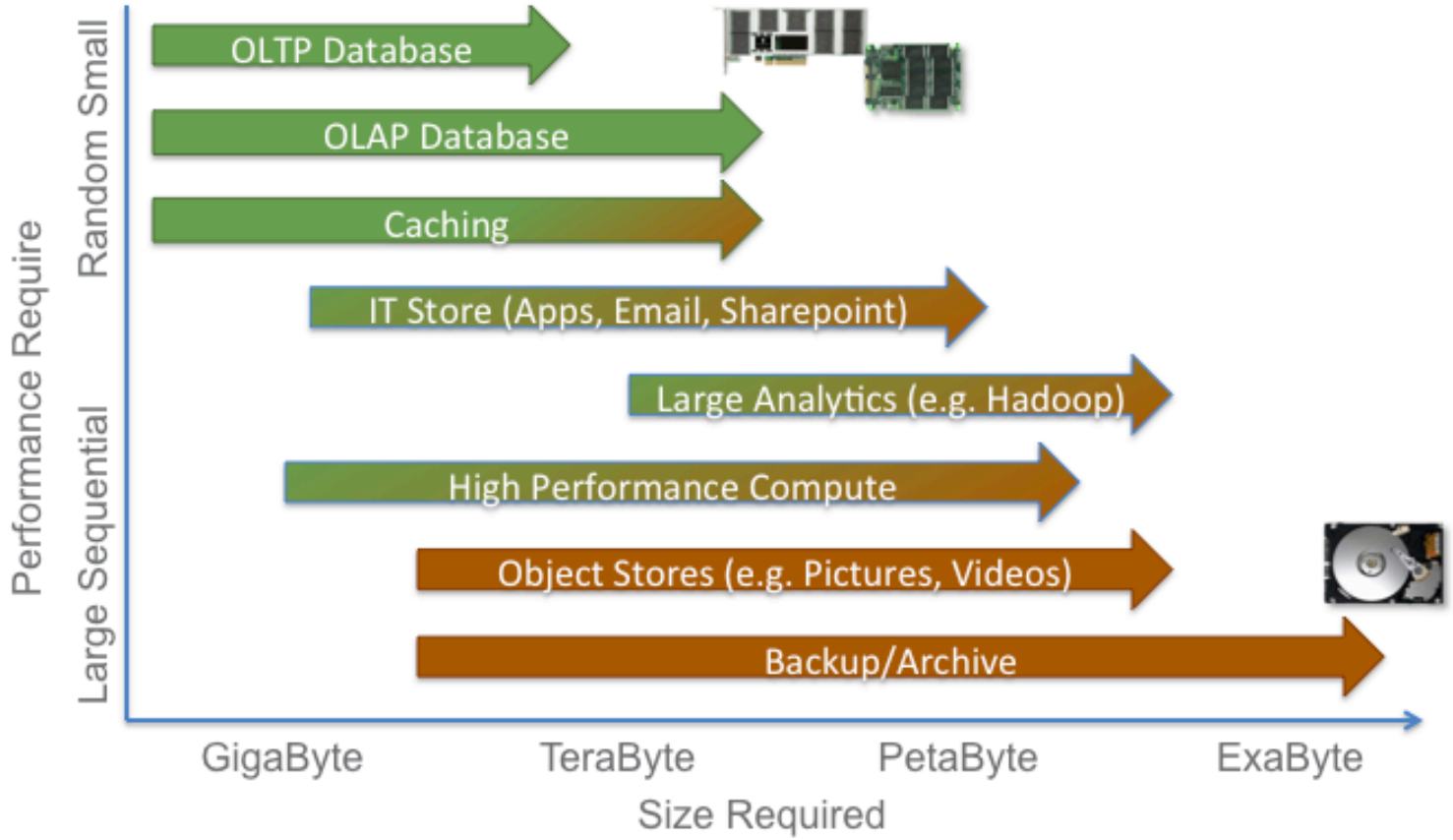
- **Application Benefits of SSD Flash**
  - **Standard CAPX/OPEX benchmarks for key applications (a.l.a. TPC-C, E, H)**



Time: 4:50 - 5:20

Open Discussion
Next Actions

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Open Discussion:

Next Actions:

- **Feedback on Kick-Off Meeting Discussion**
- **Agenda & Topics for Meeting No. 2**

Time: 5:20 - 5:30

Supplemental Slides